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10/727,157	12/02/2003	Richard Thomas Plunkett	PEA08US	6698

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EXAMINER	
CHRZANOWSKI, MATTHEW R	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,157	PLUNKETT, RICHARD THOMAS	
	Examiner	Art Unit	
	Matthew R. Chrzanowski	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/02/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. **Claim 1** includes a limitation enclosed in parentheses as follows: "(the requests are not placed anywhere, they are simply received)". It is unclear as to why applicant would use parentheses other than to indicate reference characters or to indicate optional limitations. Examiner assumes this is optional limitation.

3. Applicant is advised that should **claim 2** be found allowable, **claim 4** will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

4. **Claim 18** contains the same reference characters (a-b) as uses in claim 1. Furthermore, step (a) of claim 18 is the same as step (a) of claim 10 and

therefore appears to be a duplicated limitation. And step (b) is a completely different step from claim 18 to claim 10.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claim 1** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **Claim 1** recites the following: "(the requests are not placed anywhere, they are simply received)." It is unclear as to why applicant would use parentheses other than to indicate reference characters or to indicate optional limitations. Examiner assumes this is optional limitation. Furthermore, it is not understood how access requests can be not be placed anywhere *(even temporarily)* as it appears access requests are associated with a timeslot as disclosed in claim 1, unless the step (a) alone does not place the access request anywhere, however a subsequent step may store temporarily the access request.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. **Claim 10-16** rejected under 35 U.S.C. 102(e) as being anticipated by **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")**.

Consider **claim 10**, Stacovsky discloses a method of arbitrating between access requests from a plurality of requestors for access to a resource *(FIG. 9A-B, FIG. 14)*, wherein at least one of the requestors is defined as higher priority access to the resource *(column 8, lines 35-48)*, the method comprising the steps of:

(a) receiving a plurality of the access requests *(commands 1, 2: FIG. 14)*;

(b) in the event an access request from the at least one of the requestors is received, initiating performance of the access request in preference to the requestor as specified by the timeslot list and regardless of whether or not the at least one of the requestors is in the timeslot list *(FIFO: FIG. 14)*.

Consider **claim 11**, and as applied to **claim 10** above, Stacovsky disclose the method wherein the at least one requestor requires lower latency access to the resource than at least one of the other requestors

from which access requests can be received *(in a system with different processors and memories it is implied that that there will be access requests of varying latencies)*.

Consider **claim 12**, and as applied to **claim 10** above, Stacovsky disclose the method wherein the at least one requestor is a processor *(FIG. 9A-B, 14)*.

Consider **claim 13**, and as applied to **claim 10** above, Stacovsky disclose the method wherein the resource is a memory *(FIG. 9A-B, 14)*.

Consider **claim 14**, and as applied to **claim 10** above, Stacovsky disclose the method wherein step (b) includes the substep of performing the access request from the requestor immediately following completion of any current access request being reformed *(command 3 is executed before command 2, but immediately after command 1: FIG. 14)*.

Consider **claim 15**, and as applied to **claim 10** above, Stacovsky disclose the method wherein step (b) is performed such that a frequency of the at least one requestor being granted preferential performance of its access requests *(FIG. 14)* is limited within a time period *(In order to prevent what is referred to as livelock, a livelock counter register 156*

contains information about the number of consecutive requests (or responses) with the higher priority which can bypass requests (or responses) with a lower priority. In this way, the lower priority request (or response) can not be starved for a substantial number of clock cycles: column 8, lines 35-48; and in the case there is only one requestor making the requests and therefore only being granted preferential performance, the livelock counter registers is of the one requestor).

Consider **claim 16**, and as applied to **claim 15** above, Stacovsky disclose the method wherein early performance of access requests from the at least one requestor is restricted to a maximum number of times within a predetermined number of timeslots *(In order to prevent what is referred to as livelock, a livelock counter register 156 contains information about the number of consecutive requests (or responses) with the higher priority which can bypass requests (or responses) with a lower priority. In this way, the lower priority request (or response) can not be starved for a substantial number of clock cycles.: column 8, lines 35-48; and in the case there is only one requestor making the requests and therefore only being granted preferential performance, the livelock counter registers is of the one requestor).*

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. **Claims 1-5** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** in view of **Gray et al. (US Patent # 6816923, hereinafter "Gray")**.

Consider **claim 1**, Stacovsky discloses a method for arbitrating between a plurality of access requests issued in relation to a resource by a plurality of requesters *(FIG. 9A-B, 14)*, wherein each request can be one of at least two types, a first of the types having a higher latency associated with its performance than at least some of the other types *(it can but not necessarily does; in a system with different processors and memories it is*

implied that that there will be access requests of varying latencies), the method including the steps of:

(a) receiving a plurality of the access requests *(commands 1, 2: FIG. 14)*;

(b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*; and

(c) in the event an access request as arbitrated via the lookahead pointer, initiating performance of the access request earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot *(command 3 is executed before command 2, but after 1: FIG. 14)*.

Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention a First-in-first-out or ordered buffer allows (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*, because a use of these buffers are a well-known way of indicating order of requests to indicate priority based on order in which the entries were received. Furthermore, it would have been obvious

because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Stacovsky orders based on timeslot and prioritizes certain requests, however, Stacovsky may not specifically disclose prioritizing based on if the request **is of the first type**.

Gray discloses prioritizing higher latency access requests *(requests from a device having larger latency)* earlier than normal ordered operation *(A device having both a high priority and a low bandwidth may be able to withstand a larger latency than a device having a lower priority and a higher bandwidth: column 8, line 64—column 9, line 4)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to prioritizing based on if the request is of the first type in the system of Stacovsky, because Gray teaches a device with may be able to withstand a larger latency *(column 8, line 64—column 9, line 4)*. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Consider **claims 2 and 4**, and as applied to **claim 1** above, Stacovsky in view of Gray disclose the method wherein step (c) includes the substep of performing the access request indicated by the lookahead pointer immediately after the access request indicated by the current

pointer is performed *(Stacovsky: command 3 is executed before command 2, but immediately after command 1: FIG. 14)*.

Consider **claim 3**, and as applied to **claim 1** above, Stacovsky in view of Gray disclose the method wherein the first type of access request is a memory write request *(Stacovsky: column 9, lines 3-5; Gray: column 6, lines 63-64)*.

Consider **claim 5**, and as applied to **claim 1** above, Stacovsky in view of Gray disclose the method wherein the number of timeslots between the timeslot indicated by the lookahead pointer and the timeslot indicated by the current pointer takes into account a latency difference between performing an access request of the first type and at least one of the other access request types *(Stacovsky: the timeslots or entries "take into account" the latency difference because they arrive in order of receipt even though relative to time one of higher latency could have been sent before a lower latency time request but received by the arbiter afterwards; Gray: Furthermore, takes into account priority and latency: column 8, line 64—column 9, line 4)*.

13. **Claims 6-9** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** in view

of **Gray et al. (US Patent # 6816923, hereinafter "Gray") and Radke et al. (US Patent # 6741253 B2, hereinafter "Radke")**.

Consider **claim 6**, Stacovsky discloses an plurality of integrated circuit including: a plurality of operative units, each of which is capable of issuing a request for access to a memory accessible by the integrated circuit *(FIG. 9A-B, 14)*; and an timeslot arbitrator for arbitrating between requests issued by the operative units for access to the memory *(FIG. 14)*, wherein each request can be one of at least two types, a first of the types having a higher latency associated with its performance than at least some of the other types *(it can but not necessarily does; in a system with different processors and memories it is implied that that there will be access requests of varying latencies)*, the timeslot arbitrator being configured to:

(a) receiving a plurality of the access requests *(commands 1, 2: FIG. 14)*;

(b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*; and

(c) in the event an access request as arbitrated via the lookahead pointer, initiating performance of the access request

earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot *(command 3 is executed before command 2, but after 1: FIG. 14)*.

Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention a First-in-first-out or ordered buffer allows (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*, because a use of these buffers are a well-known way of indicating order of requests to indicate priority based on order in which the entries were received. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Stacovsky orders based on timeslot and prioritizes certain requests, however, Stacovsky may not specifically disclose the entire device is an integrated circuit and prioritizing based on if the request **is of the first type**.

Gray discloses prioritizing higher latency access requests *(requests from a device having larger latency)* earlier than normal ordered operation *(A device having both a high priority and a low bandwidth may be able to withstand a larger latency than a device having a lower priority and a higher bandwidth: column 8, line 64—column 9, line 4)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to prioritizing based on if the request is of the first type in the system of Stacovsky, because Gray teaches a device with may be able to withstand a larger latency *(column 8, line 64—column 9, line 4)*. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Furthermore, Radke discloses placing processors and memory on an embedded/integrated circuit *(column 1, lines 14-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made integrate the entire processors, memory and arbitrator in the system of Stacovsky, because it is a design choice which increases throughput of processed data because the processors are closer to the memory. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Consider **claim 7**, and as applied to **claim 6** above, Stacovsky in view of Gray and Radke disclose the integrated circuit wherein the first type of access request is a memory write request *(Stacovsky: column 9, lines 3-5; Gray: column 6, lines 63-64)*.

Consider **claim 8**, and as applied to **claim 7** above, Stacovsky in view of Gray and Radke disclose the integrated circuit wherein the integrated circuit includes a memory interface unit operatively connected with, and under the control of, the timeslot arbitrator *(FIG. 9A-B, FIG. 14)*, and wherein the memory interface is operatively connected to: one or more of the operative units via one or more communications buses *(FIG. 9A-B, FIG. 14)*.

Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention that the memory via a memory bus can be of greater width than the communications buses, because it a design choice of which a smaller bus size can be cheaper and easier to manufacture because of less bus lines. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Consider **claim 9**, and as applied to **claim 6** above, Stacovsky in view of Gray and Radke disclose the integrated circuit wherein the number of timeslots between the timeslot indicated by the lookahead pointer and the timeslot indicated by the current pointer takes into account a latency difference between performing an access request of the first type and at least one of access request types *(Stacovsky: the timeslots or entries "take into account" the latency difference because they arrive in order of receipt even though relative to time one of higher latency could have been*

sent before a lower latency time request but received by the arbiter afterwards; Gray: Furthermore, takes into account priority and latency: column 8, line 64—column 9, line 4).

14. **Claim 17** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** as applied to **claim 10** above, and further in view of **Radke et al. (US Patent # 6741253 B2, hereinafter "Radke")**.

Consider **claim 17**, and as applied to **claim 10** above, Stacovsky disclose the method wherein the requesters are hardware units and the method is implemented by a timeslot arbitrator *(FIG. 9A-B, 14)*.

However, Stacovsky may not specifically disclose wherein the requesters and time slot arbitrator are on an integrated circuit.

Radke discloses placing processors, memory, and memory controllers on an embedded/integrated circuit *(column 1, lines 14-30)*.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made integrate the entire processors, memory and arbitrator in the system of Stacovsky, because it is a design choice which increases throughput of processed data because the processors are closer to the memory. Furthermore, it would have been

obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

15. **Claim 18** rejected under 35 U.S.C. 103(a) as being unpatentable over **Stacovsky et al. (US Patent # 6526484 B1, hereinafter "Stacovsky")** as applied to **claim 10** above, and further in view of **Gray et al. (US Patent # 6816923, hereinafter "Gray")**.

Consider **claim 18**, as applied to **claim 10** above, Stacovsky discloses the method wherein each request can be one of at least two types, a first of the types having a higher latency associated with its performance than at least some of the other types *(it can but not necessarily does; in a system with different processors and memories it is implied that that there will be access requests of varying latencies)*, the method including the steps of:

(a) receiving a plurality of the access requests *(commands 1, 2: FIG. 14)*;

(b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*; and

(c) in the event an access request as arbitrated via the lookahead pointer, initiating performance of the access request earlier than the position in the list suggests it would be performed should it be started when the current pointer reached the timeslot *(command 3 is executed before command 2, but after 1: FIG. 14)*.

Examiner is taking official notice that it would have been obvious to one of ordinary skill in the art at the time of the invention a First-in-first-out or ordered buffer allows (b) maintaining a current pointer that points to a current timeslot in a timeslot list, and at least one lookahead pointer that points to a future timeslot in the timeslot list *(FIFO and ordered buffers maintain a current pointer and future or last received pointer to signify the last entry in the queue)*, because a use of these buffers are a well-known way of indicating order of requests to indicate priority based on order in which the entries were received. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Stacovsky orders based on timeslot and prioritizes certain requests, however, Stacovsky may not specifically disclose prioritizing based on if the request **is of the first type**.

Gray discloses prioritizing higher latency access requests *(requests from a device having larger latency)* earlier than normal ordered operation *(A device having both a high priority and a low bandwidth may be able to*

withstand a larger latency than a device having a lower priority and a higher bandwidth: column 8, line 64—column 9, line 4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to prioritizing based on if the request is of the first type in the system of Stacovsky, because Gray teaches a device with may be able to withstand a larger latency *(column 8, line 64—column 9, line 4)*. Furthermore, it would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew R. Chrzanowski whose telephone number is (571) 270-1176. The examiner can normally be reached on M-Th 7:30am-5:00pm, Every other Friday 7:30am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew R Chrzanowski
Examiner
Art Unit 2186

09/27/2007
/MC/

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